AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-2. (Cancelled)

3. (Currently amended) ~~The wire load estimating method as claimed in claim 2~~ A wire load estimating method comprising;

reading a netlist;

generating connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

dividing an area of a chip into two or more regions and determining connection point coordinates for each of said regions using said connection information and locations of said instances as placed, the connection point coordinates of at least one of the regions being center coordinates of said region, wherein the center coordinates ~~of each of said regions~~ are calculated by adding ~~the~~ top right vertex coordinates of ~~each of~~ said ~~regions~~ region to ~~the~~ bottom left vertex coordinates of ~~each of~~ said ~~regions~~ region and dividing the result of the addition by 2;

determining a wiring path using said connection point coordinates; and

estimating a wire capacitance value and a wire reisistance value with reference to said wiring path.

4. (Cancelled).

5. (Currently amended) ~~The wire load estimating method as claimed in claim 4~~ A wire load estimating method comprising:

reading a netlist;

generating connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

dividing an area of a chip into two or more regions and determining connection point coordinates for each of said regions using said connection information and locations of said instances as placed, the connection point coordinates of at least one of the regions being pin coordinates of the macro blocks located within said regions, wherein the pin coordinates of said macro block which is rotated or mirror-imaged are calculated ~~by the use of~~ using ~~the~~ bottom left vertex coordinates of said macro block in a base condition, ~~the~~ location of said pin coordinates relative to the bottom left vertex coordinates, and at least one of transformation types of rotation and mirror-imaging;

determining a wiring path by the use of said connection point coordinates; and

estimating a wire capacitance value and a wire reisistance value with reference to said wiring path.

6. (Currently amended) ~~The wire load estimating method as claimed in claim 1~~ A wire load estimating method comprising:

reading a netlist;

generating connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

dividing an area of a chip into two or more regions and determining connection point coordinates for each of said regions using said connection information and locations of said instances as placed, wherein said connection point coordinates are calculated ~~by the use of~~ using ~~the~~ bottom left vertex coordinates of said regions, indications of ~~the~~ top side, ~~the~~ bottom side, ~~the~~ right side or ~~the~~ left side of said regions on which the respective connection points are located, ~~the~~ vertical or horizontal size of said regions, and ~~the~~ coordinates of ~~the~~ connection points of two or more instances;

determining a wiring path by the use of said connection point coordinates; and

estimating a wire capacitance value and a wire reisistance value with reference to said wiring path.

7. (Currently amended) ~~The wire load estimating method as claimed in claim 1~~ A wire load estimating method comprising:

reading a netlist;

generating connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

dividing an area of a chip into two or more regions and determining connection point coordinates for each of said regions using said connection information and locations of said instances as placed;

determining a wiring path using said connection point coordinates by:

calculating ~~the~~ a maximum value and ~~the~~ a minimum value of ~~the~~ x-coordinates, ~~as well as those of~~ and ~~the~~ y-coordinates, of a plurality of ~~the~~ connection points which are connected to a same signal;

calculating ~~the~~ a difference between the maximum value and the minimum value of said x-coordinates ~~as well as those of~~ and said y-coordinates, and judging which side in the x-direction or the y-direction of a rectangular region including said connection points is longer than the other with reference to said differences;

arranging a root wire in the direction along the longer side;

connecting said root wire to ~~the~~ a farthest one of said connection points from said root wire by means of a connection wire between the farthest connection point and the root wire; and ~~then~~

connecting, by means of a connection wire, each of the remaining points of said connection points to ~~the wire~~ either another one of the connection wires or the root wire, whichever is closest ~~which is one of said connection wires and said root wire and located closest to said each of the remaining points in a sequence from a closest connection point from said root wire~~; and

estimating a wire capacitance value and a wire reisistance value with reference to said wiring path.

8. (Cancelled).

9. (Currently amended) ~~The wire load estimating method as claimed in claim 1~~ A wire load estimating method comprising:

reading a netlist;

generating connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

dividing an area of a chip into two or more regions and determining connection point coordinates for each of said regions using said connection information and locations of said instances as placed;

determining a wiring path using said connection point coordinates;

estimating a wire capacitance value and a wire reisistance value with reference to said wiring path;

wherein a temporary repeater cell is inserted on the basis of the wire capacitance value and the wire resistance value; and wherein

the respective instances are placed on the basis of the result of inserting the temporary repeater cell.

10.-12.(Cancelled).

13. (Currently amended) ~~The computer program product for claim 12, wherein the computer readable program code for causing the computer to determine connection point coordinates calculates the center coordinates of each of said regions~~

A computer program product for estimating a wire load comprising:

instructions configured to read a netlist;

instructions configured to generate connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

instructions configured to divide an area of a chip into two or more regions;

instructions configured to determine connection point coordinates for at least one of the regions by calculating center coordinates of the region by adding ~~the~~ top right vertex coordinates of ~~each of~~ said ~~regions~~ region to ~~the~~ bottom left vertex coordinates of ~~each of~~ said ~~regions~~ region and dividing the result of the addition by 2;

instructions configured to determine a wiring path by the use of said connection point coordinates; and

instructions configured to estimate a wire capacitance value and a wire resistance value with reference to said wiring path.

14. (Cancelled).

15. (Currently amended) ~~The computer program product for claim 14, wherein the computer readable program code for causing the computer to determine connection point coordinates calculates the pin coordinates of said macro block which is rotated or mirror-imaged~~ A computer program product for estimating a wire load comprising:

instructions configured to read a netlist;

instructions configured to generate connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

instructions configured to divide an area of a chip into two or more regions;

instructions configured to determine connection point coordinates for at least one of the regions by using pin coordinates of a rotated or mirror-imaged macro block which is located within said regions by ~~the use of the~~ using bottom left vertex coordinates of said macro block in a base condition, ~~the~~ location of said pin coordinates relative to the bottom left vertex coordinates, and at least one of transformation types of rotation and mirror-imaging;

instructions configured to determine a wiring path by the use of said connection point coordinates; and

instructions configured to estimate a wire capacitance value and a wire resistance value with reference to said wiring path.

16. (Currently amended) ~~The computer program product for claim 11, wherein the computer readable program code for causing the computer to determine connection point coordinates calculates said connection point coordinates~~ A computer program product for estimating a wire load comprising:

instructions configured to read a netlist;

instructions configured to generate connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

instructions configured to divide an area of a chip into two or more regions;

instructions configured to determine connection point coordinates for at least one of said regions by ~~the use of the~~ using bottom left vertex coordinates of said ~~regions~~ region, indications of ~~the~~ top side, ~~the~~ bottom side, ~~the~~ right side or ~~the~~ left side of said ~~regions~~ region on which the respective connection points are located, ~~the~~ vertical or horizontal size of said ~~regions~~ region, and ~~the~~ coordinates of the connection points of two or more instances;

instructions configured to determine a wiring path by the use of said connection point coordinates; and

instructions configured to estimate a wire capacitance value and a wire resistance value with reference to said wiring path.

17. (Currently amended) ~~The computer program product for claim 11, wherein the computer readable program code for causing the computer to determine connection point coordinates comprises:~~ A computer program product for estimating a wire load comprising:

instructions configured to read a netlist;

instructions configured to generate connection information including names of signals, identification names and names of pins of instances which include cells, macro blocks and synthesized blocks as described in said netlist;

instructions configured to divide an area of a chip into two or more regions and determining connection point coordinates for each of said regions by the use of said connection information and locations of said instances as placed;

instructions configured to determine a wiring path using said connection point coordinates by:

~~a computer readable program code for causing the computer to calculate~~ calculating ~~the~~ a maximum value and ~~the~~ a minimum value of ~~the~~ x-coordinates~~, as well as those of~~ and ~~the~~ y-coordinates~~,~~ of a plurality of the connection points which are connected to a same signal;

~~a computer readable program code for causing the computer to calculate~~ calculating ~~the~~ a difference between the maximum value and the minimum value of said x-coordinates~~, as well as those of~~ and said y-coordinates, and judging which side in the x-direction or the y-direction of a rectangular region including said connection points is longer than the other with reference to said differences;

~~a computer readable program code for causing the computer to arrange~~ arranging a root wire in the direction along the longer side;

~~a computer readable program code for causing the computer to connect~~ connecting said root wire to ~~the~~ a farthest one of said connection points from said root wire by means of a connection wire between the farthest connection point and the root wire; and ~~then~~

~~a computer readable program code for causing the computer to connect~~ connecting, by means of a connection wire, each of the remaining points of said connection points to either another one of the connection wires or the root wire, whichever is closest ~~the wire which is one of said connection wires and said root wire and located closest to said each of the remaining points in a sequence from a closest connection point from said root wire;~~ and

instructions configured to estimate a wire capacitance value and a wire resistance value with reference to said wiring path.

18. (Cancelled).

19. (Currently amended) ~~The computer program product for claim 11, further including~~ A computer program product for estimating a wire load comprising:

instructions configured to read a netlist;

instructions configured to generate connection information including names of signals, identification names and names of pins of instances, wherein the instances include cells, macro blocks and synthesized blocks as described in said netlist;

instructions configured to divide an area of a chip into two or more regions and determining connection point coordinates for each of said regions using said connection information and locations of said instances as placed;

instructions configured to determine a wiring path using said connection point coordinates;

instructions configured to estimate a wire capacitance value and a wire resistance value with reference to said wiring path; and

~~a computer readable program code for causing the computer~~ instructions configured to insert a temporary repeater cell on the basis of the wire capacitance value and the wire resistance value; and

~~a computer readable program code for causing the computer~~ instructions configured to place the respective instances on the basis of the result of inserting the temporary repeater cell.

20. (Cancelled).

21. (New) The wire load estimating method of claim 7, wherein the step of connecting, by means of a connection wire, each of the remaining points of said connection points is executed in a sequence from the farthest connection point from said root wire to a closest connection point from said wire.

22. (New) The computer program product for estimating a wire load of claim 17, wherein the step of connecting, by means of a connection wire, each of the remaining points of said connection points in the instructions configured to determine a wiring path using said connection point coordinates is executed in a sequence from the farthest connection point from said root wire to a closest connection point from said wire.